IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Johns et al.**	§	Group Art Unit: **2181**
	§	
Serial No. **10/809,553**	§	Examiner: **Lee, Chun Kuan**
	§	
Filed: **March 25, 2004**	§	Customer No. **50170**
	§	
For: **Method to Provide Cache Management Commands for a DMA Controller**	§	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S REPLY BRIEF (37 C.F.R. 41.41)

This reply brief is in response to the Examiner's Answer mailed November 14, 2007.

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447.

I. Response to Examiner's Remarks Regarding Rejection Under 35 U.S.C. 102

Appellants argued that the *Futral* reference does not mention the word "cache," and *Futral* does not describe a memory that behaves as a cache; therefore, one cannot interpret the memory of *Futral* to be a cache. The Examiner's Answer states:

> In accordance to Appellant's own definition of a cache "[a] cache is a storage that keeps frequently accessed data or program instructions readily available so that the device, in this case a DAM controller, does not access them repeatedly from a slower storage." Additionally, in accordance to Appellant's disclosure, in the Abstract of the application, "a cache can be a system cache or a DMA cache."
>
> The examiner respectfully disagree and maintains that Futral's teaching of a memory in a computer system does allow for frequent and rapid access of data in a fashion substantially similar to the Appellant's claim language regarding a cache. Both the Appellant's language and Futral's memory teach the access of data via memory. Furthermore, the definition of a cache is considered among other things a system memory and therefore Futral's memory, which is directly related to a computer system, reads on applicant's claimed langauge.

Appellants note that the rejection based on *Futral* relies heavily on the Examiner's interpretation of the reference in this case. The Examiner has made interpretations of the reference to establish a *prima facie* case of anticipation. If these interpretations are incorrect, or if the interpretations still fail to account for every claim feature, then, simply put, the reference fails to anticipate the claims.

In this case, the Examiner interprets the memory in *Futral* to be equivalent to a cache, as recited in claim 1. The Examiner uses language from Appellants' own specification to argue that any system memory can be interpreted to be a cache. Appellants respectfully disagree. This clearly amounts to warping the definitions of the terms in the claims to be broad enough to read on the reference. However, Appellants submit that a person of ordinary skill in the art would never interpret the term "cache" to mean "a system memory" as the Examiner's Answer attempts to do.

Furthermore, the Examiner's Answer argues that the claim language and the language of *Futral* can be interpreted such that they are "in a fashion substantially similar." However, "substantially similar" is not the standard for anticipation. Appellants submit that the Office has not established a *prima facie* case of anticipation, because *Futral* clearly fails to teach a cache.

Appellants argued that *Futral* does not teach DMA commands for performing cache management operations. The Examiner's Answer states:

> The examiner respectfully disagrees and maintains that Futral's the DMA operation to be associated with cache management operation, such as management the data transferring operation to/from the cache. Therefore, Futral does teach a DMA controller that is configured to execute the DMA commands for the management of a cache.

Appellants respectfully disagree that *Futral* teaches DMA commands for management of a cache, because *Futral* makes no mention whatsoever of a cache. The Examiner's response to the argument is pure contradiction and begs the question. If Futral makes no mention of a cache, how can Futral possibly teach special DMA commands to be executed by a DMA controller for the management of a cache?

II. Response to Examiner's Remarks Regarding Rejection Under 35 U.S.C. 103

Appellants argue that the remaining references, *Ollivier*, *Liao*, and *Ohba* also fail to teach or suggest a DMA controller that is configured to execute DMA commands for cache management. The Examiner's Answer acknowledges that *Ollivier*, *Liao*, and *Ohba* are not relied upon for the argued features. Therefore, if *Futral* does not teach a cache or a DMA controller that is configured to execute DMA commands for cache management, than any combination of *Futral* with *Ollivier*, *Liao*, and/or *Ohba* also cannot teach these features.

III. Conclusion

In view of the above, Appellants respectfully submit that claims 1-21 of the present application are not taught or suggested by the applied references. Accordingly, Appellants request that the Board of Patent Appeals and Interferences overturn the rejections set forth in the Final Office Action.

Respectfully submitted,

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